A bidirectional, sinusoidal, high-frequency inverter design

E.Koutroulis, J.Chatzakis, K.Kalaitzakis and N.C.Voulgaris

Abstract: A new method for the design of a bidirectional inverter based on the sinusoidal pulse-width modulation principle and the use of a low-cost and lightweight ferrite-core transformer is presented. The inverter is designed for either ohmic or inductive loads. In the case of inductive loads the reactive power is transferred back to the DC input power source using a new active rectifier design. The inverter is controlled by two minimum-time feedback loops, providing relatively low output voltage distortion (less than 2% for DC input higher than 24V) and good load regulation (better than 2%), while the inverter efficiency remains relatively constant (from 80 to 85%) over a wide output power range (75 to 200W) and DC input voltage range (23 to 28V). Theoretical results are experimentally verified using a laboratory prototype.

1 Introduction

DC/AC power converters (inverters) are widely used today mainly in uninterruptible power supply systems, AC motor drives, induction heating and renewable energy source systems. The simplest form of an inverter is the bridge-type [1], shown in Fig. 1*a*, where a power bridge is controlled according to the sinusoidal pulse-width modulation (SPWM) principle and the resulting SPWM wave is filtered to produce the alternating output voltage. This method has the disadvantage that in the case where low direct input voltage is used, the power transformer required is of large size, heavy weight and high cost. An inverter design method based on the use of a converter to convert the direct input voltage to rectified sine wave and a power bridge to produce the alternating output voltage [2], shown in Fig. 1*b*, has the disadvantage of not providing galvanic isolation between the DC input source and the load.

In many applications it is important for an inverter to be of relatively small size and lightweight. This can be achieved by using a high-frequency (HF) link inverter topology. A popular HF link inverter topology is the so-called DC/DC converter type, Fig. 2*a*. In this scheme [3], a bridge inverter is used to convert the direct input voltage into an HF square wave, which, in turn, is rectified and filtered. The lowpass filter output is a high-level direct voltage that is converted into a low-frequency wave by an SPWM inverter. In an alternative version, the HF bridge inverter produces an HF PWM wave, thus reducing the transformer losses [4, 5].

In the last two design methods the power flow is unidirectional from the DC input source to the AC output load because of the diode rectifier. However, in applications involving renewable energy source systems where energy is stored in batteries, it is desirable to have a bidirectional power flow. This is also important in the case of reactive loads, where the reactive power must be transferred back to the DC input source to increase the overall system efficiency. The implementation of bidirectional power flow by connecting a flyback converter at the output of a DC/DC converter type inverter [6] to transfer the reactive power back to the DC input source results in increased output voltage distortion due to the delay associated with the reactive power sensing and control.

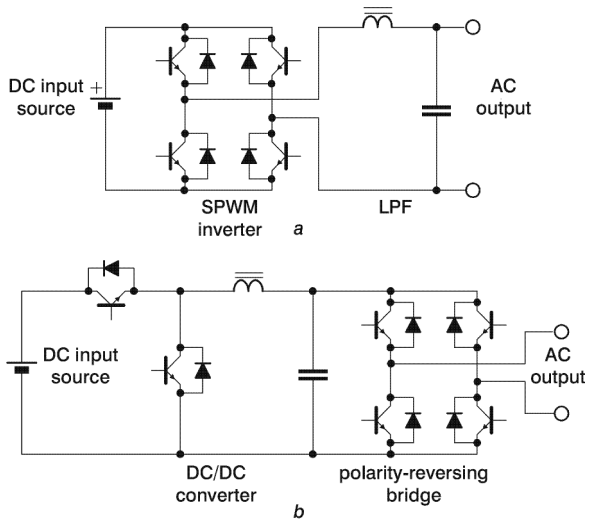

Fig. 1 *Low-frequency inverter design methods*
a Bridge-type inverter
b Inverter design consisting of a DC/DC converter and power bridge

The most common inverter topology featuring bidirectional power flow is the HF link with a cycloconverter output stage [7, 8], shown in Fig. 2*b*. This method has the drawback that the cycloconverter power semiconductors operate at high frequency, thus having high switching losses and high cost.

An alternative method for achieving bidirectional power flow is proposed, Fig. 2*c*. An HF bridge inverter produces a 50Hz modulated SPWM HF wave whose voltage level is boosted by an HF transformer. An active rectifier rectifies

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The authors are with the Department of Electronics and Computer Engineering, Technical University of Crete, GR-73100, Chania, Greece

the resulting wave. The rectifier topology used permits reverse current flow to the DC input source in case of an inductive load. A polarity-reversing bridge at the rectifier output reverses the polarity of the second half 50Hz period rectified pulses thus producing an SPWM wave. A lowpass output filter produces a 50Hz, high-voltage and low-distortion sinusoidal wave. The switching rate of the polarity-reversing bridge is determined by the low output-voltage frequency (50Hz) so that it has low switching losses and low cost.

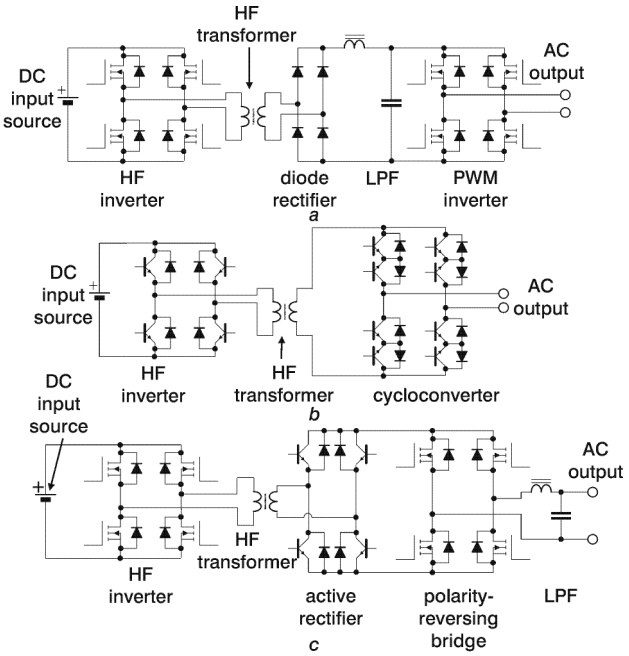

Fig. 2 *HF link inverter topologies*
a DC/DC converter type high-frequency link inverter
b HF link inverter with cycloconverter output stage
c Block diagram of proposed inverter

The proposed system is a low-cost, small-size, lightweight and high-efficiency inverter with low output-voltage distortion, designed for both ohmic and inductive loads.

2 Description

A more detailed diagram of the proposed system is shown in Fig. 3, while the principal voltage waveforms at different stages of the DC/AC conversion are shown in Fig. 4. With reference to Fig. 3, the feedback-loop reference signal of the inverter is a constant-amplitude, low-distortion, crystal-controlled sine wave (50Hz). This signal is produced as shown in Fig. 5. The waveform Fig. 5*c* is half the difference

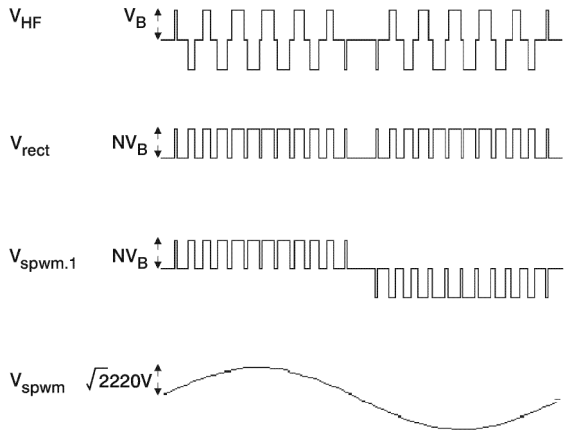

Fig. 4 *Principal waveforms at different stages of DC/AC conversion*

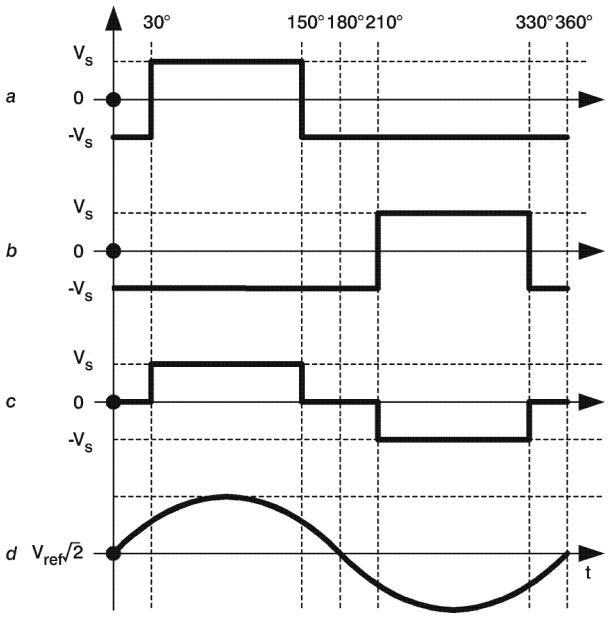

Fig. 5 *Production of 50 Hz sinusoidal reference signal*

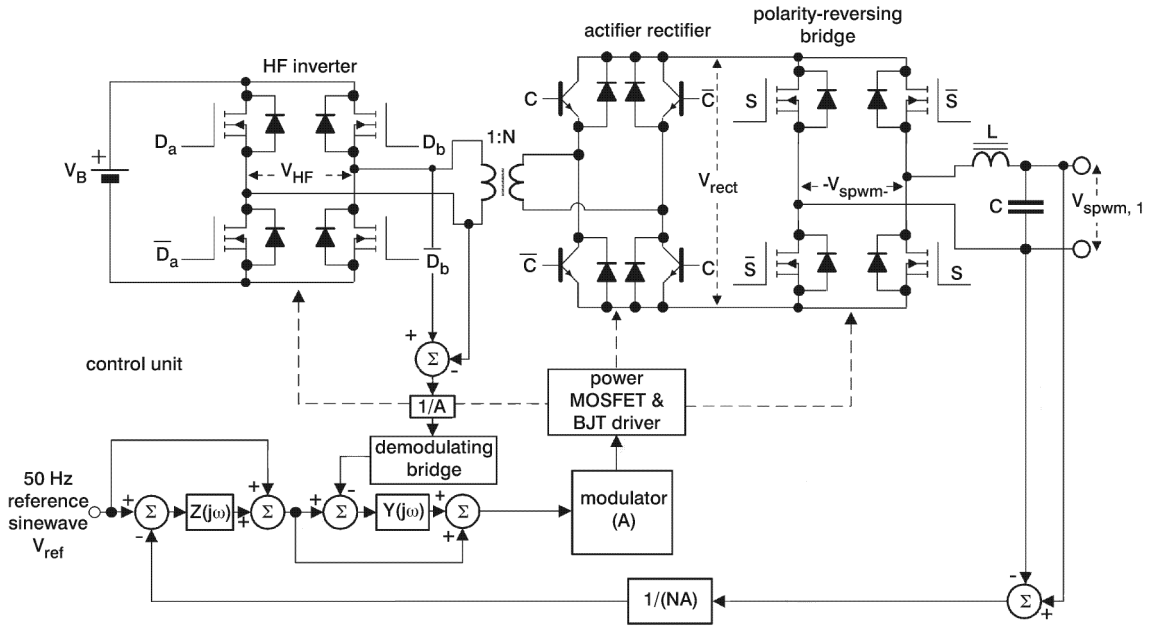

Fig. 3 *Detailed block diagram of proposed inverter*

of the 50Hz waveforms Figs. 5*a* and *b*, which are produced from a crystal-controlled CMOS logic circuit. This waveform does not contain second, third and fourth harmonics [9], so a lowpass filter with a cut-off frequency well above 50 Hz is adequate to produce a low-distortion reference sine wave, Fig. 5*d*. If the CMOS output stage of the logic circuit that produces the 50Hz waveforms Figs. 5*a* and *b* is powered by a stable symmetric direct supply voltage $\pm V_s$, the produced pulses are rail-to-rail and the produced sine-wave has a stable amplitude with an RMS value V_{ref} given by

$$V_{ref} = \frac{4V_s}{\sqrt{2}\pi}\cos 30^\circ \qquad (1)$$

where V_s is the peak voltage of the 50Hz pulse waveforms shown in Fig. 5*a*. The advantages of this method are:

• high accuracy of the produced waveform frequency due to the crystal

• low sensitivity of the output voltage to the circuit component values; because the cut-off frequency of the lowpass filter is not critical compared with the filter required for a 50Hz square-wave oscillator, where a good quality band-pass filter would be needed

• the produced voltage amplitude is very stable compared with other oscillator types (e.g. Wien bridge oscillator) because it depends only on the logic circuit supply voltage, and

• a good quality three-phase reference sine wave oscillator can be easily implemented using this method, if the case of a three-phase inverter implementation is considered.

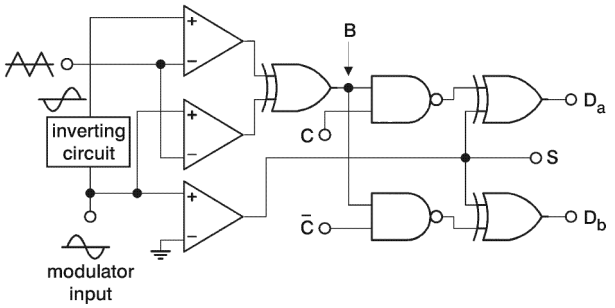

Fig. 6 *Modulator control unit diagram*

The modulator control unit shown in Fig. 6 operates according to the SPWM technique. The associated waveforms are shown in Fig. 7. The amplitude of the triangular wave is made proportional to the DC input voltage level to minimise modulator gain variations caused by input voltage variations. The modulation index m_a is defined as

$$m_a \equiv \frac{\sqrt{2}V_{ref}}{V_{tr}} = \frac{\sqrt{2}V_{ref}}{V_B/A} = A\frac{\sqrt{2}V_{ref}}{V_B} \qquad (2)$$

where V_{tr} is the peak voltage of the triangular wave, A is the modulator gain and V_B is the direct input voltage. The modulator gain A is selected such that, when the input voltage V_B is at its minimum design value, the modulation index is unity. The wave at point B shown in Fig. 7*a* is a full-wave rectified SPWM pulse-train [10], while the control signal *C*, shown in Fig. 7*b* is used to alternatively split the rectified SPWM wave pulses. This HF control signal is produced by the previously mentioned logic circuit, which also produces the 50Hz reference sine wave. The resulting control signals are combined with the sign waveform *S* of the modulator input Fig. 7*c* and drive the two sides of the HF inverter illustrated in Fig. 3 [signals D_a and D_b in Fig. 7*d* and *e*, respectively] thus producing the HF wave of Fig. 7*f* (V_{HF} in Fig. 4]. This wave has an equivalent harmonic profile similar to the difference of two SPWM waves carrying the same modulated signal with their carriers having 180° phase difference. It consists of pulses with amplitude equal to the power supply voltage and zero DC and low-frequency components. A blocking capacitor (not shown in the diagram) is used in the HF inverter output to eliminate any DC offset signal. The demodulating bridge Fig. 3, consists of four analogue switches and is used to convert the HF inverter output into a 50Hz SPWM wave for the implementation of the inner feedback loop.

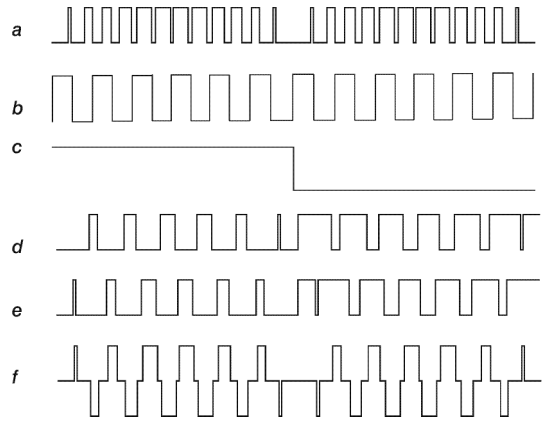

Fig. 7 *Waveforms*
a Rectified SPWM wave *S*
b Wave *C*
c Sign of modulator input
d Wave D_a
e Wave D_b
f HF inverter output

A ferrite-core, step-up transformer boosts the voltage level of the modulator output pulses to the required level Fig. 3. The active-rectifier is a full-wave bridge with each side consisting of a diode which conducts when active power is transferred from the DC input power source to the load and a parallel-connected NPN power transistor which conducts when reactive power is transferred from the load to the DC power source, in the case of an inductive load. The transistors are switched on and off during the zero-voltage time interval between the high-frequency modulation signal pulses and are driven by the control signal *C*, shown in Fig. 7*b*. A small inductor in parallel with a resistance forming an *RL* snubber is placed in series with the transformer output to minimise any overvoltages between the HF transformer high-voltage side terminals, caused by the HF transformer leakage inductance. A similar *RL* snubber is placed at the active rectifier output to reduce any adverse effects to the power transformer output waveform caused by the parasitic capacitances of the polarity-reversing bridge power switches. Both of these snubbers are not shown in Fig. 3 to simplify the diagram.

The polarity-reversing bridge operates at a 50Hz rate and is switched during the zero output voltage interval thus having negligible switching losses. The polarity-reversing bridge power switches are controlled by the sign waveform of the modulator input Fig. 7*c* and its output is an SPWM wave. The RMS value of the fundamental-frequency component of this SPWM wave $V_{spwm,1}$ is

$$V_{spwm,1} = \frac{m_a N V_B}{\sqrt{2}} = \frac{A\sqrt{2}V_{ref}NV_B}{\sqrt{2}V_B} = ANV_{ref} \qquad (3)$$

where N is the transformer turns ratio. An LC network at the output of the polarity-reversing bridge forms a lowpass filter, which eliminates all high-order harmonics from the SPWM wave so that the inverter output is a 50Hz low-

distortion, 220 V_{RMS} sinusoidal wave. The LC filter resonant frequency f_c is calculated such that the output total harmonic distortion (THD) is less than 5%. Simulation runs show that if f_c is kept below the 1/25th of the inverter switching frequency f_s and the modulation index is 0.65, the THD is kept below 3.25%. The filter inductor value L is calculated such that the voltage drop across the inductor is less than 3% of the inverter output voltage, i.e.

$$I_{load,max} 2\pi f L < 0.03 V_{ac} \tag{4}$$

where $I_{load,max}$ is the maximum RMS load current, V_{ac} is the RMS output voltage and f is the output frequency (50Hz). The filter capacitor value C is calculated from the resonance relation

$$C = \frac{1}{(2\pi f_c)^2 L} \tag{5}$$

Because the frequency f_c is much higher than f, the capacitor impedance is much higher than the load impedance

$$|Z_C| = \frac{1}{2\pi f C} \gg |Z_{load}| \tag{6}$$

where Z_c is the filter capacitor impedance and Z_{load} is the load impedance.

The power transformer turns ratio is calculated using the inverter model shown in Fig. 8, so that when the minimum specified load impedance $Z_{load,min}$ is applied, the inverter output voltage, neglecting snubber effects, is within its specifications, i.e.

$$V_{ac,min} = V_{spwm,1} - \frac{V_{ac,min}}{Z_{load,min}}(N^2 r_{mod} + r + j\omega L) \tag{7}$$

where $V_{ac,min}$ is the minimum specified output voltage, r_{mod} is the modulator internal output resistance and r is the equivalent of the transformer internal resistance, the output inductor resistance and the power MOSFET's series resistance.

The inverter is controlled by an inner and an outer minimum-time (feedforward) feedback loop as shown in Fig. 8, thus achieving good output voltage regulation and low distortion. A minimum-time type feedback control loop has the advantage of providing zero steady-state offset error [11] and fast dynamic response. The feedback loops are phase and amplitude compensated so that the system is absolutely stable under any practical ohmic or inductive loading conditions. The design principle adopted is that the exact component characteristics cannot be specified so a worst-case design method was employed. The inverter closed-loop transfer function is given by

$$H(s) = \frac{V_o(s)}{V_{ref}(s)} = \frac{A^2 N[Z(s)+1][Y(s)+1]G(s)}{1 + AY(s) + AZ(s)[Y(s)+1]G(s)} \tag{8}$$

where:

$$G(s) = \frac{Z_{load}}{\left\{Z_{load}\frac{L}{2}Cs^2 + \left[\frac{L}{2} + (r + r_{mod})Z_{load}C + Z_{LRC}Z_{load}C\right]s + Z_{LRC} + Z_{load} + r + r_{mod}\right\}}$$

$$Z_{LRC} = \frac{LC_s s^2 + 4R_s C_s s + 4}{LC_s s^2 + 2R_s C_s s + 2} \cdot \frac{L}{2} s$$

The inner loop compensation network has been designed so that the loop gain is unity at the output filter resonance frequency. Thus oscillations of the system are suppressed, even under malfunction conditions (i.e. increase of the modulator internal output resistance). The transfer function of the inner loop is

$$Y(j\omega) = K_i \frac{1 + \frac{j\omega}{\omega_{iz}}}{\left(1 + \frac{j\omega}{\omega_{ip1}}\right)\left(1 + \frac{j\omega}{\omega_{ip2}}\right)} \quad \text{for } \omega_{ip1} < \omega_{iz} < \omega_{ip2} \tag{9}$$

where K_i is the low-frequency gain, ω_{ip1}, ω_{ip2} are the design poles and ω_{iz} is the design zero. The lowest pole ω_{ip1} is placed close to the first harmonic of the alternating output voltage frequency, and K_i is determined so that the loop gain is reduced to unity for frequency values below the LC output filter resonance frequency. The zero–pole pair ω_{iz} – ω_{ip2} is used to increase the loop bandwidth to eliminate the distortion due to the dead-time effect [12] and asymmetry of the modulator bridge, thus improving the modulator linearity. In addition, ω_{ip2} suppresses the switching frequency residuals.

The outer loop reduces the output voltage distortion caused by the transformer, the active rectifier and the polarity reversing bridge. The outer loop compensation network transfer function is given by the following equation:

$$Z(j\omega) = K_o \frac{1 + \frac{j\omega}{\omega_{oz}}}{1 + \frac{j\omega}{\omega_{op}}} \quad \text{for } \omega_{op} < \omega_{oz} \tag{10}$$

where K_0 is the low-frequency gain, ω_{op} and ω_{oz} are the design pole and zero, respectively. The pole ω_{op} is placed near the output voltage frequency and K_0 is determined so that the loop gain is close to unity for frequency values

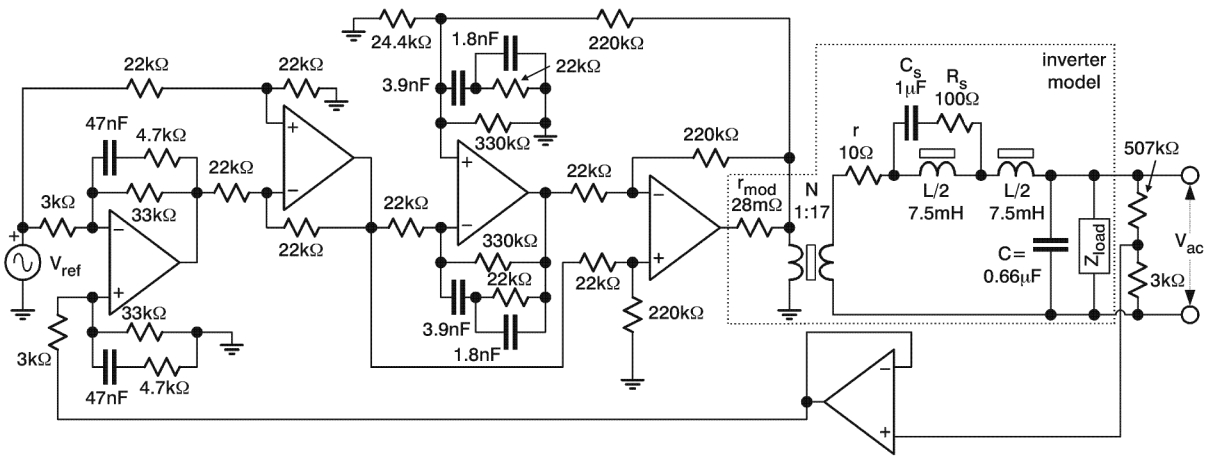

Fig. 8 *SPICE inverter model*

below the LC filter resonance frequency. Additionally, an RC snubber (R_s and C_s in Fig. 8), is used to reduce the LC filter quality factor so that two distinct poles appear and the phase variations become smoother. The zero ω_{oz} is placed below the lowest expected pole of the combination of the LC filter and inverter load. The inverter may also operate with capacitive loads, but in such a case the compensation has to be modified to assure system stability.

Low-cost, off-the-shelf electronic components are used throughout the design. The modulator switching bridge and the polarity-reversing bridge are built around n-channel power MOSFETs that have the advantage of simple driving requirements and high switching speed. The rectifier bridge is built around fast switching diodes and bipolar junction transistors, since these components have lower output parasitic capacitance compared with lower-speed MOSFETs. The high-voltage side active components are operating under constant duty-cycle conditions and can be easily driven by only two transformers (each with multiple secondary-windings), one for each bridge. The power transformer is wound on an E55/21 ferrite core and is a low-cost, lightweight and high-efficiency type. The transformer switching frequency is set at 25kHz, but this frequency may be increased for higher output power rating without seriously affecting the transformer efficiency. The frequency of 25kHz is a compromise of factors such as power semiconductor switching losses and cost, and transformer size, weight and losses.

3 Theoretical and experimental results

A laboratory prototype of the inverter was constructed according to the previously described methodology with the following specifications:

- Sinusoidal output voltage 220–230VRMS, 50Hz
- Maximum output power 250W with low distortion (THD < 2%) for DC inputs equal to or higher than 24V.
- Input voltage source in the range of 23–28V (24V nominal voltage provided by batteries).

The HF inverter bridge is built around the IRFZ44 power MOSFETs, the active rectifier diodes are of PFR856 type, while the BJTs used are the BUV56A. The polarity-reversing bridge is built around the IRF840 power MOSFETs. The inverter design parameters calculated by eqns. 4, 5 and 7 for $f_s = 2 \times 25.6$kHz are: output filter inductor L = 15mH, output filter capacitor C = 0.66μF, modulator gain A = 10 and transformer turns ratio N = 19.

Inverter stability was verified by simulation using a SPICE program. Amplitude and phase Bode diagrams of the inner control-loop gain with the outer loop disconnected are shown in Fig. 9*a*, while amplitude and phase Bode plots of the outer-loop gain with the inner-loop in operation under no-load and full-load conditions are shown in Figs. 9*b* and *c*, respectively.

The simulated output voltage transient behaviour for a step change to the amplitude of the reference voltage, which corresponds to a change of the inverter output voltage from 110 to 220V_{rms}, is illustrated in Fig. 10*a*, while the inverter output voltage behaviour for a change to the output load from 0W to 220W is depicted in Fig.10*b*. It is

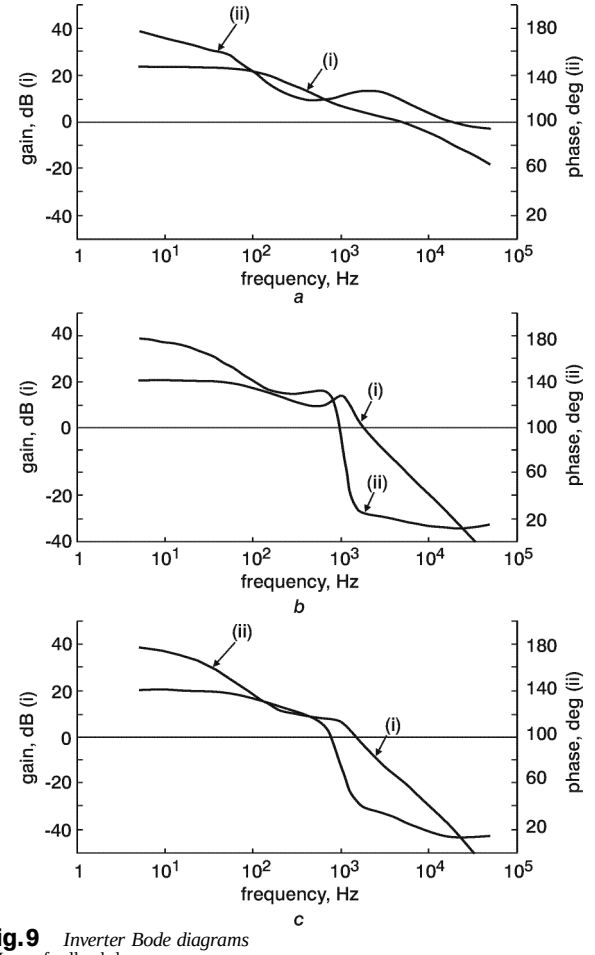

Fig. 9 *Inverter Bode diagrams*
a Inner feedback loop
b Both control loops closed under no-load condition
c Both control loops closed under full-load condition

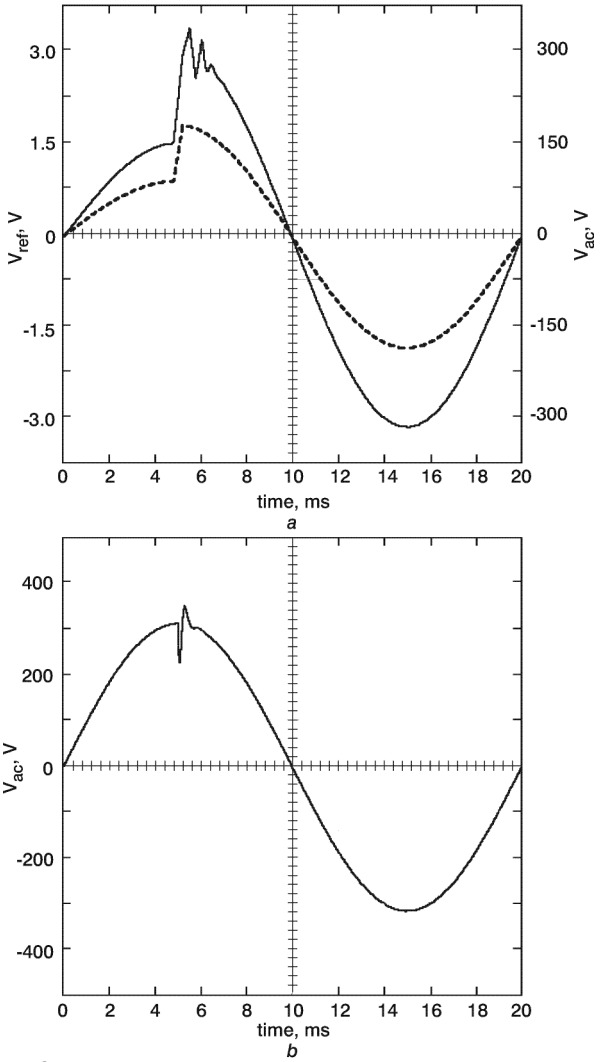

Fig. 10 *Simulated output voltage transient behaviour*
a step change to amplitude of the reference voltage
——— V_{ac}; – – – – V_{ref}
b step change to output load from 0 to 220W

observed that the settling time is below 5ms in both cases, which is easily manipulated by overvoltage protection circuits.

The inverter efficiency η is defined as

$$\eta \equiv \frac{P_o}{P_o + P_L} \tag{11}$$

where P_o is the output power and P_L is the total power loss. The partial power losses across the inverter stages are

control unit power consumption

$$P_C = I_C V B (\simeq 10\ \mathrm{W})$$

inverter total ohmic losses $P_R = I_{load}^2 (N^2 r_{mod} + r)$

modulator MOSFET switching losses

$$P_S = \frac{1}{2} N V B I_{load} (t_{on} + t_{off}) \frac{f_s}{2}$$

rectifier diode conduction losses $P_D = V_F I_{load}$

magnetic component's losses

$$P_M = K_h f_s B_{max}^z + K_e f_s^2 B_{max}^2 \tag{12}$$

where: t_{on}, t_{off} are the on and off delay times, V_F is the diode conduction voltage drop, K_h, K_e are constants depending on the magnetic material, z is Steinmetz's constant and B_{max} is the flux density's maximum value. The polarity-reversing bridge switching losses due to zero-voltage switching are neglected. The power transistor conduction losses are neglected assuming ohmic load, while their switching losses due to zero-voltage switching are neglected.

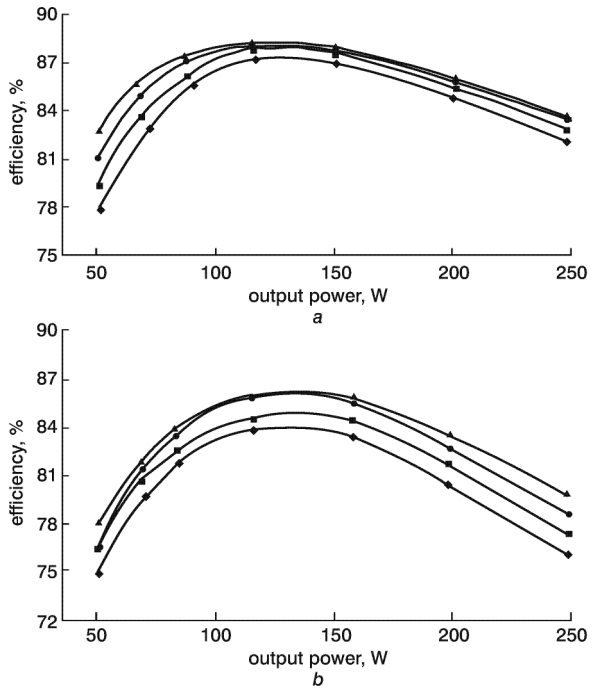

Fig. 11 *Inverter efficiency for various input voltages*
a Theoretical efficiency
b Measured efficiency
—▲— 23V —■— 26V
—●— 24V —◆— 28V

The inverter theoretical efficiency as a function of the output power for various input voltages is shown in Fig. 11*a*, while its measured efficiency with ohmic loads is shown in Fig. 11*b*. The efficiency does not change substantially with the input voltage, since it remains within 5% for more than 20% variation (23 to 28V) as the load varies from 75 to 200W. It is also observed that the efficiency decreases as the input voltage increases at any output power level. This is caused by increased switching losses of the modulator and the active-rectifier devices and the losses in the snubber networks, when the input voltage rises. The measured efficiency is 2–3% lower than the theoretical efficiency because of the higher ohmic and switching losses of the laboratory-built inverter.

The measured output voltage THD variation with ohmic loads and various input voltages is shown in Fig. 12. The output voltage THD is less than 1.4% for any input voltage and for output power less than 150W. It remains below 1.6% as the output power increases to 250W, except for the case of discharged batteries where at the level of 23V the output voltage starts to clip and the THD reaches the 5% level, still within the inverter specifications.

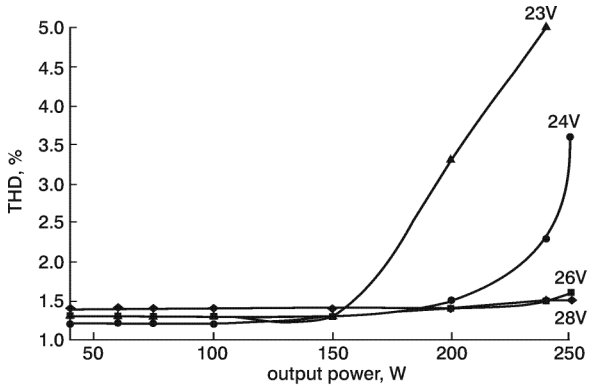

Fig. 12 *Inverter output THD for various input voltages*

Load regulation was also measured over the entire input voltage range and was found to be approximately 2% at 250W. From both theoretical calculations and simulation runs, the sensitivity of the voltage regulation with respect to the transformer ratio N is found to be 10%, with respect to the inductor value L is calculated to be 0.2% under full load conditions (worst case), and with respect to the capacitor value C is negligible.

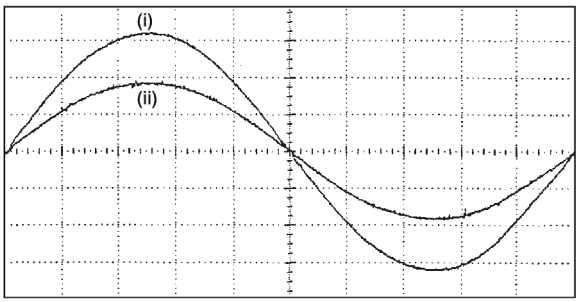

Fig. 13 *Output voltage and current with ohmic load*
Input voltage 26V, output power 250W; scales: output voltage 100V/div, output current 0.83A/div; Time 2ms/div
(i) Output voltage
(ii) Output current

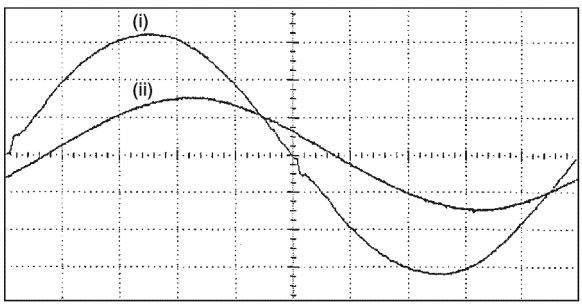

Fig. 14 *Output voltage and current with inductive load*
Input voltage = 24V, real power absorbed by the load = 114W and power factor = 0.9; scales: output voltage 100V/div; output current 0.5A/div; time 2ms/div
(i) Output voltage
(ii) Output current

The output voltage and current waveforms with ohmic load (input voltage 26V, output power 250W) are shown in

Fig. 13. The inverter efficiency is 78.7% and the output voltage THD is 1.6%. The output voltage and current waveforms with an inductive load (input voltage 24V, real power absorbed by load 114W, and power factor 0.9) are shown in Fig. 14. Under this load condition, the efficiency is 84.6% and the output THD is 2.4%.

4 Conclusions

A new method has been presented for designing low-cost and lightweight sinusoidal power inverters. They can produce low-distortion output voltage (THD less than 2% for DC input equal to or higher than 24V), good load regulation (better than 2%) and relatively high efficiency (from 80 to 85%) over a wide output power range (75 to 200W). The inverters can operate over an input voltage range from 23 to 28V. The output frequency may be easily adjusted over a wide range (in applications requiring line voltages of 50, 60 or 400Hz), since the operation of the transformer and the switching bridges is independent of the reference sine wave frequency. In addition, in the case of an inductive load, the reactive power is transferred back to the DC input source.

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