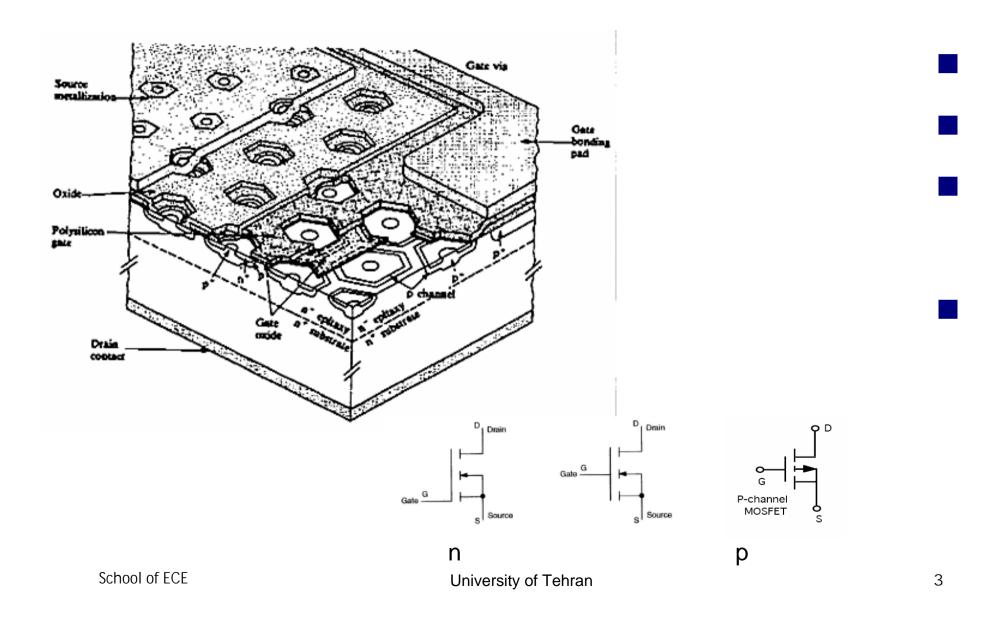
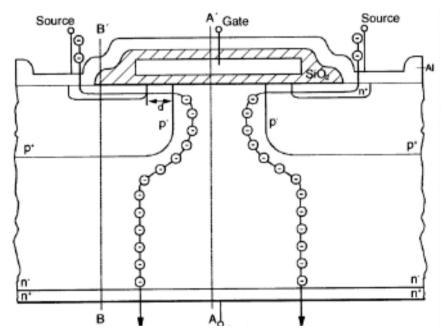
# Power MOSFET



Internation	•	•		
VMOS	•			
	LSI :			
	:			

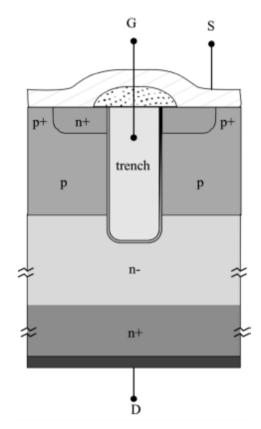






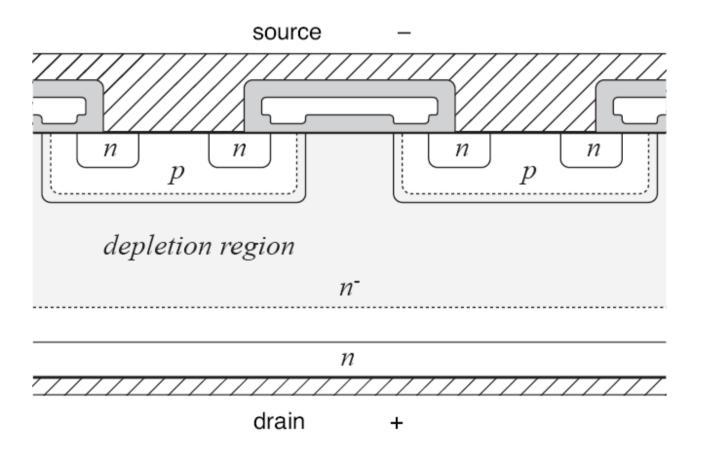
Power MOSFET (SIPMOS planar gate structure)

d: length of channel



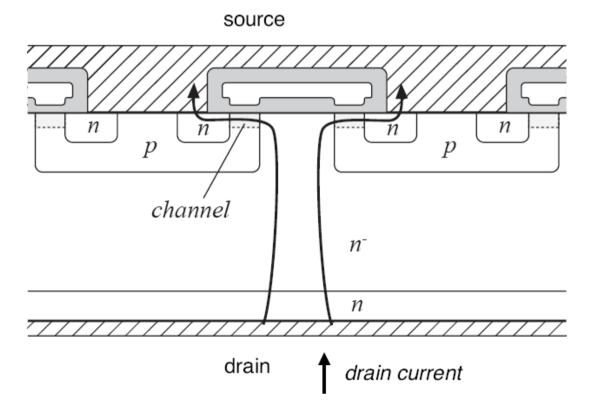
c) MOSFET with trench gate structure





- p-n<sup>-</sup> junction is reverse-biased
- off-state voltage appears across n<sup>-</sup> region





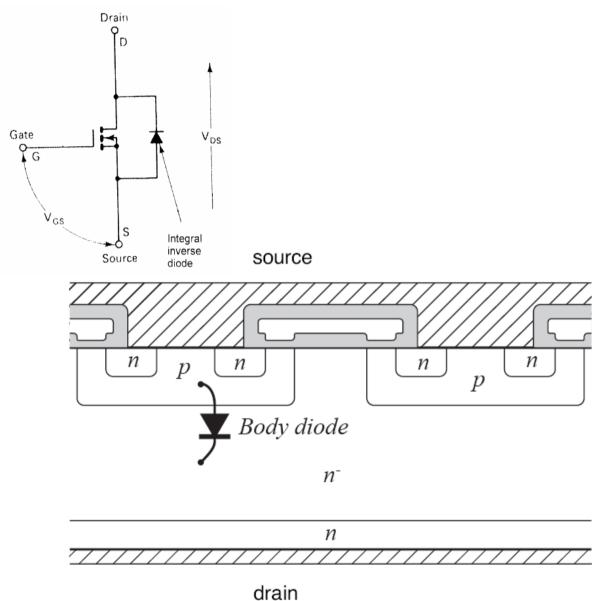
- p-n<sup>-</sup> junction is slightly reversebiased
- positive gate voltage induces conducting channel
- drain current flows through n<sup>-</sup> region and conducting channel
- on resistance = total resistances of n<sup>-</sup> region, conducting channel, source and drain contacts, etc.

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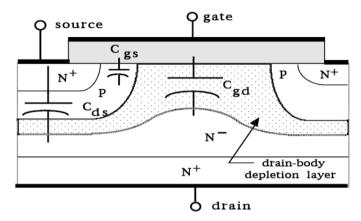
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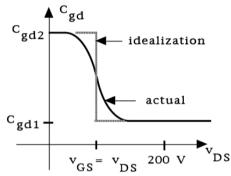


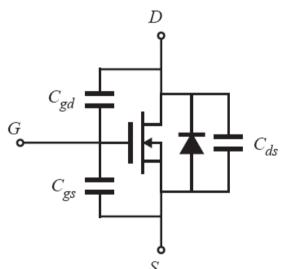


- p-n<sup>-</sup> junction forms an effective diode, in parallel with the channel
- negative drain-tosource voltage can forward-bias the body diode
- diode can conduct the full MOSFET rated current
- diode switching speed not optimized —body diode is slow, Q<sub>r</sub> is large







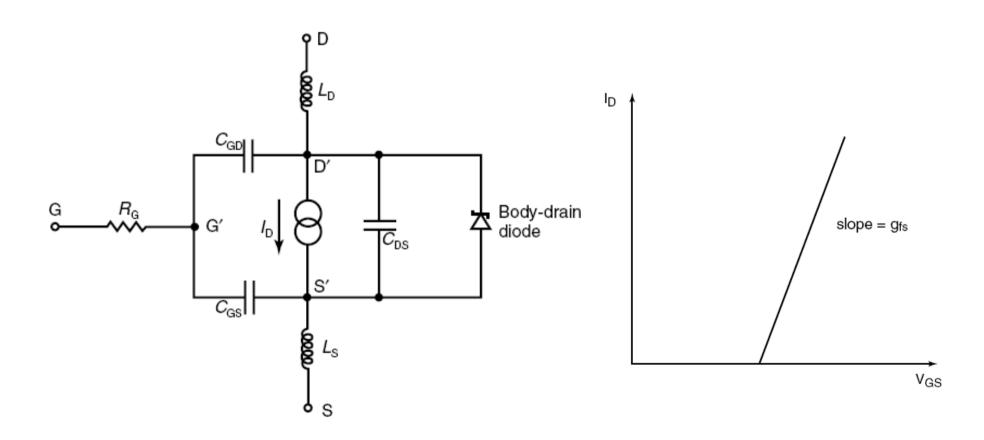


- $C_{gs}$ : large, essentially constant
- $C_{gd}$ : small, highly nonlinear
- $C_{ds}$ : intermediate in value, highly nonlinear
- · switching times determined by rate at which gate driver charges/discharges  $C_{\it gs}$  and  $C_{\it gd}$

$$C_{ds}(v_{ds}) = \frac{C_0}{\sqrt{1 + \frac{v_{ds}}{V_0}}} \qquad C_{ds}(v_{ds}) \approx C_0 \sqrt{\frac{V_0}{v_{ds}}} = \frac{C_0'}{\sqrt{v_{ds}}}$$

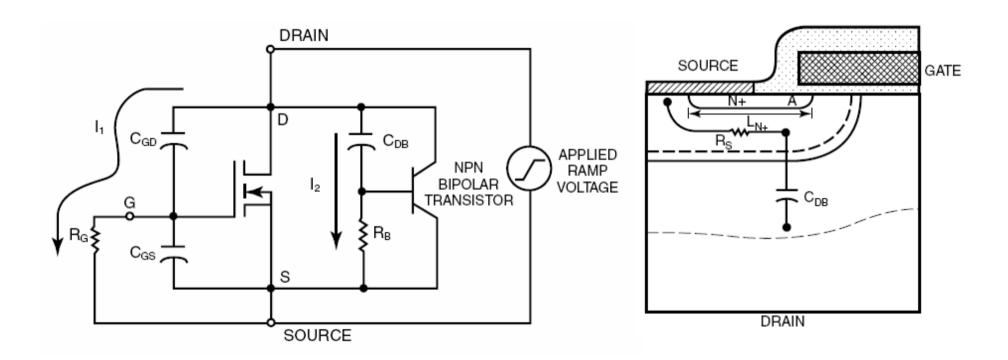
$$C_{ds}(v_{ds}) \approx C_0 \sqrt{\frac{V_0}{v_{ds}}} = \frac{C_0'}{\sqrt{v_{ds}}}$$







# dV/dt

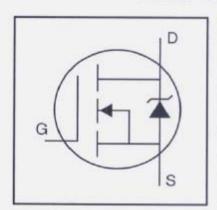




- A majority-carrier device: fast switching speed
- Typical switching frequencies: tens and hundreds of kHz
- On-resistance increases rapidly with rated blocking voltage
- Easy to drive
- The device of choice for blocking voltages less than 500V
- 1000V devices are available, but are useful only at low power levels (100W)
- Part number is selected on the basis of on-resistance rather than current rating



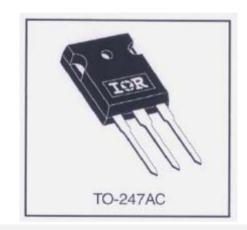
#### HEXFET® Power MOSFET



$$V_{DSS} = 100V$$

$$R_{DS(on)} = 0.036W$$

$$I_D = 42A$$



#### **Absolute Maximum Ratings**

	Parameter	Max.	Units
$I_D @ T_C = 25^{\circ}C$	Continuous Drain Current, V <sub>GS</sub> @ 10V	42	
$I_D @ T_C = 100^{\circ}C$	Continuous Drain Current, V <sub>GS</sub> @ 10V	30	A
DM	Pulsed Drain Current ①⑤	140	
P <sub>D</sub> @T <sub>C</sub> = 25°C	Power Dissipation	160	W
	Linear Derating Factor	1.1	W/°C
V <sub>GS</sub>	Gate-to-Source Voltage	± 20	V

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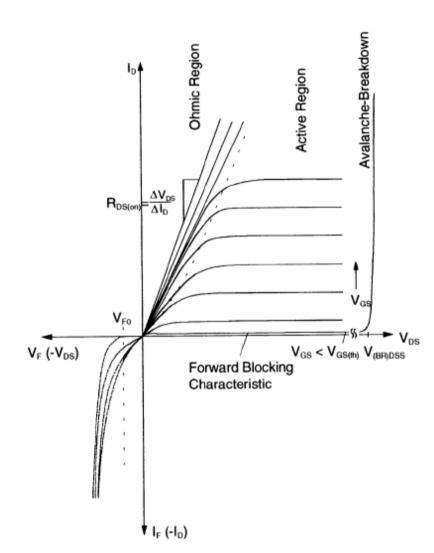
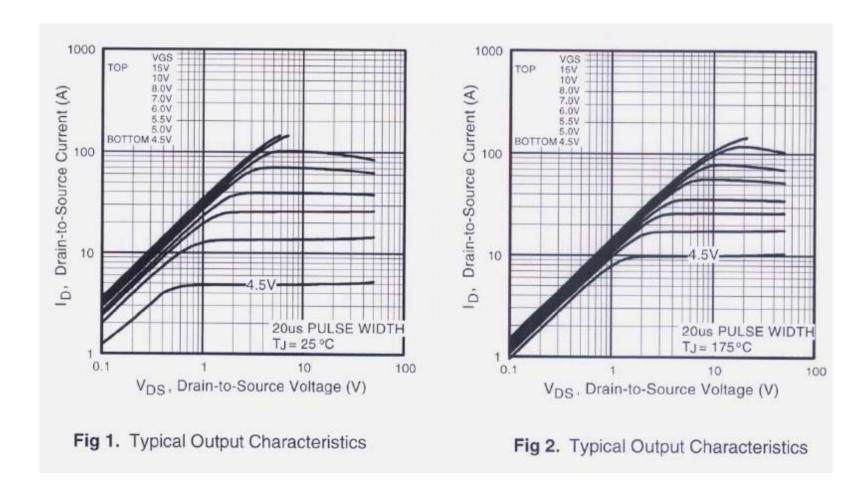


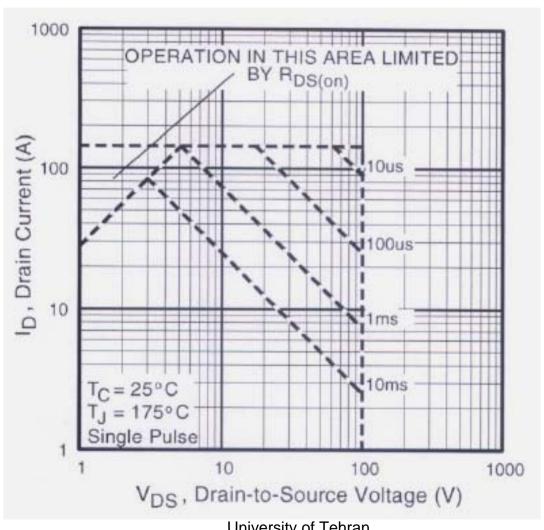
Fig. 3 a) Output characteristic of MOSFETs
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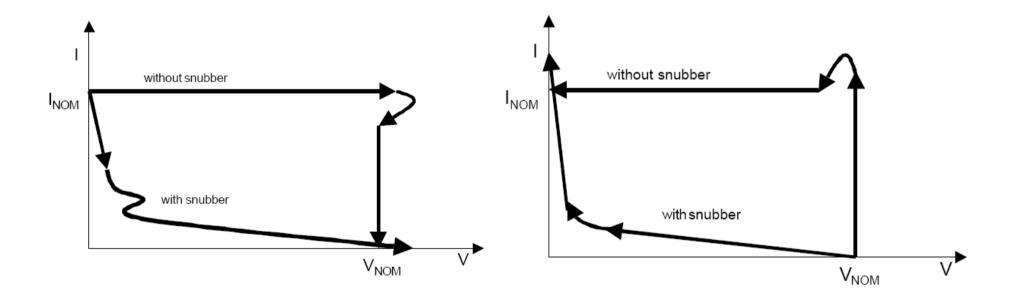
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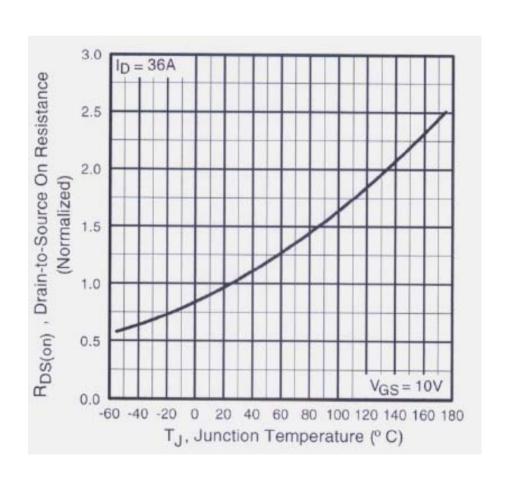
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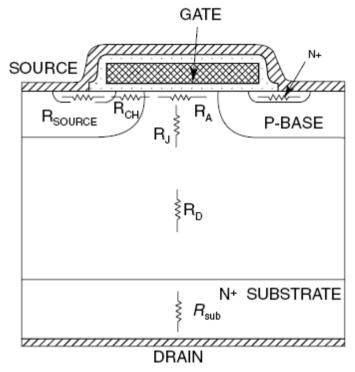






# $-\,R_{DS(on)}$

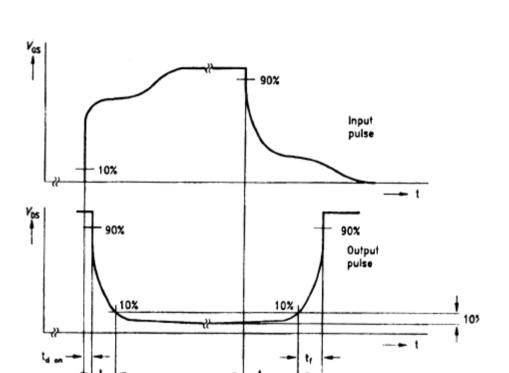


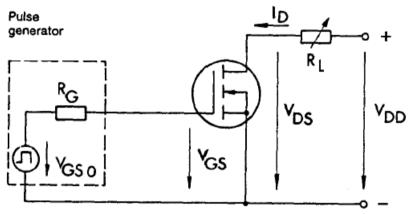


The origin of the internal resistances in a power MOSFET.

$$R_{dson} = R_{source} + R_{ch} + R_A + R_J + R_D + R_{sub} + R_{wcml}$$

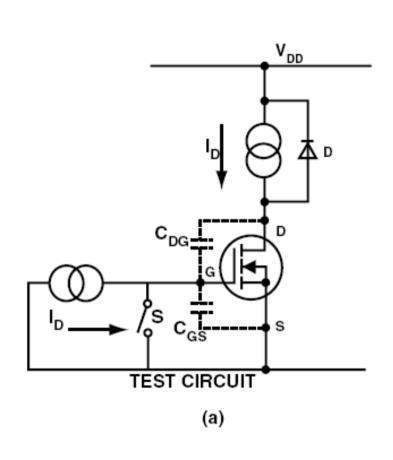


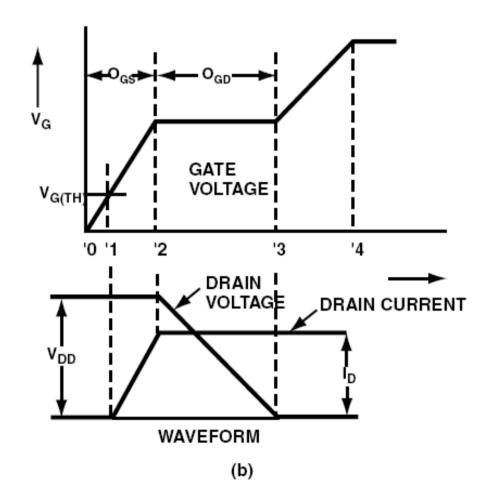




			V	-	
Turn-On Delay Time		11	-		$V_{DD} = 50V$
Rise Time	_	56	_	ne	I <sub>D</sub> = 22A
Turn-Off Delay Time	_	45	_	115	R <sub>G</sub> = 3.6W
Fall Time		40	-		R <sub>D</sub> = 2.9W, See Fig. 10 @\$
	Turn-On Delay Time Rise Time Turn-Off Delay Time	Turn-On Delay Time — — — — — — — — — — — — — — — — — — —	Turn-On Delay Time         —         11           Rise Time         —         56           Turn-Off Delay Time         —         45	Turn-On Delay Time         —         11         —           Rise Time         —         56         —           Turn-Off Delay Time         —         45         —	Turn-On Delay Time       —       11       —         Rise Time       —       56       —         Turn-Off Delay Time       —       45       —

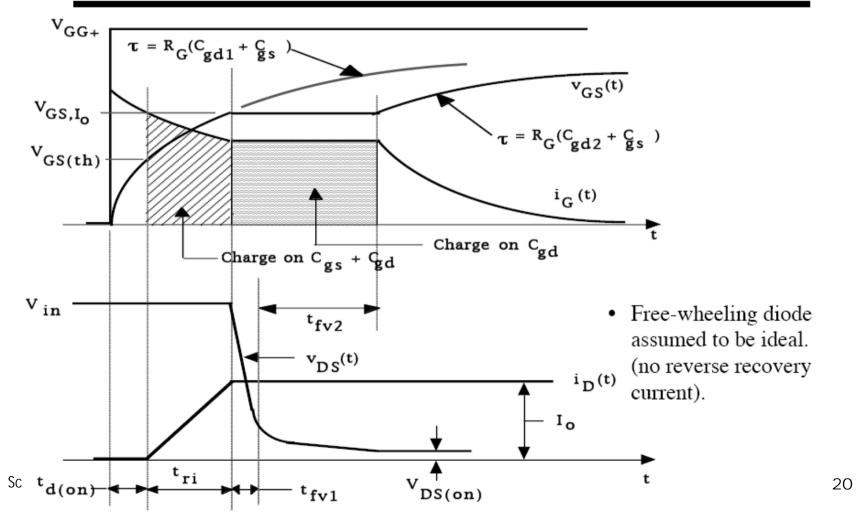






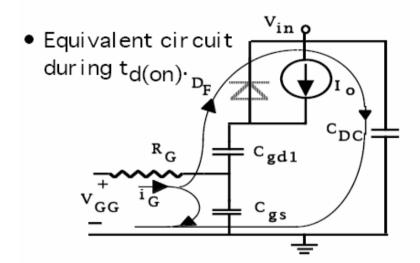
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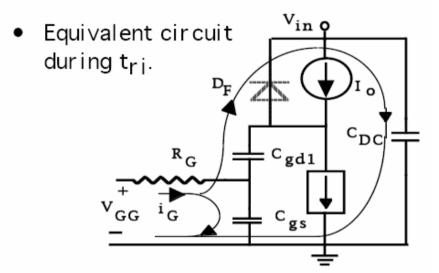
# MOSFET-based Buck Converter Turn-on Waveforms



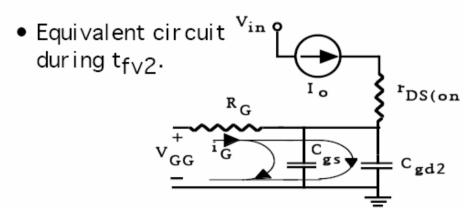
# 100

# Turn-on Equivalent Circuits for MOSFET Buck Converter



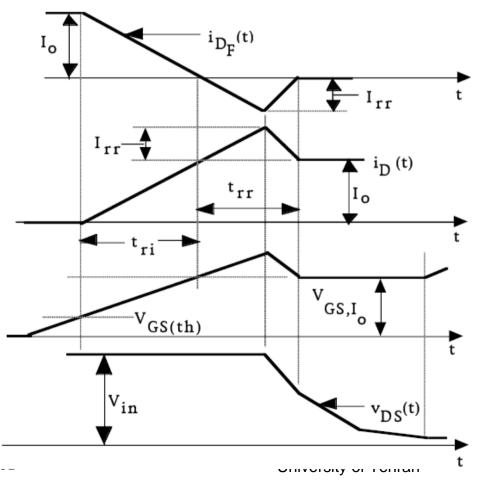


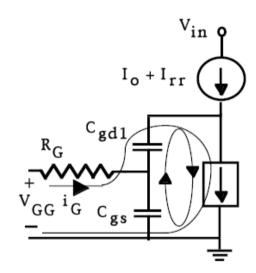
• Equivalent circuit during t<sub>fv1</sub>.



# M

# Turn-on Waveforms with Non-ideal Free-wheeling Diode



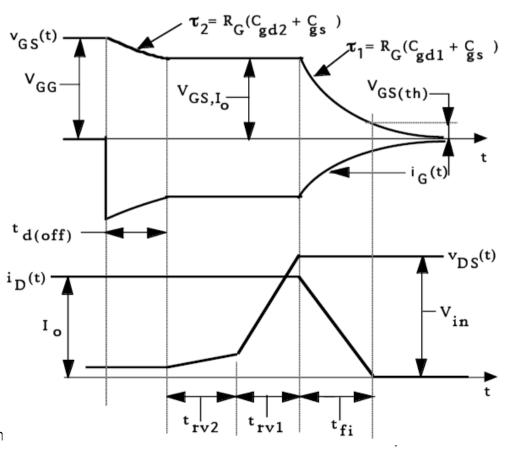


 Equivalent circuit for estimating effect of freewheeling diode reverse recovery.

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# MOSFET-based Buck Converter Turn-off Waveforms



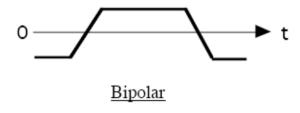
- Assume ideal freewheeling diode.
- Essentially the inverse of the turn-on process.
- Model quanitatively using the same equivalent circuits as for turn-on. Simply use correct driving voltages and initial conditions

# **Drive Circuit Design Considerations**

- · Drive circuit topologies
  - · Output signal polarity unipolar or bipolar
  - · AC or DC coupled
  - · Connected in shunt or series with power switch
- · Output current magnitude
  - Large I<sub>m</sub> shortens turn-on time but lengthens turn-off delay time
  - Large  $I_{\text{off}}$  shortens turn-off time but lengthens turn-on delay time

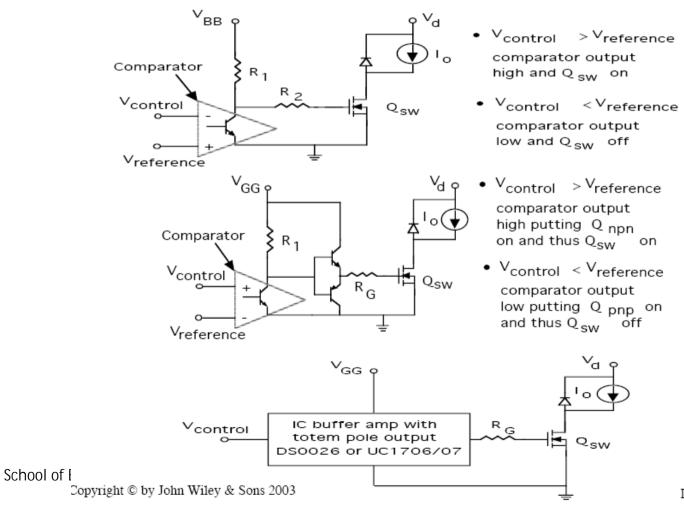


- · Provisions for power switch protection
  - · Overcurrents
  - · Blanking times for bridge circuit drives
- · Waveshaping to improve switch performance
  - Controlled di<sub>B</sub>/dt for BJT turn-off
  - · Anti-saturation diodes for BJT drives
  - · Speedup capacitors
  - · Front-porch/backporch currents



Component layout to minimize stray inductance and shielding from switching noise

#### **Unipolar DC-coupled Drive Circuits- MOSFET examples**





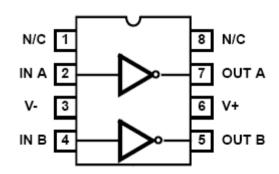
# ICL7667

#### **Dual Power MOSFET Driver**

#### **Features**

- Fast Rise and Fall Times Typically 20ns with1000pF Load
- ♦ Wide Supply Range: V<sub>DD</sub> = 4.5V to 17V
- Low Power Consumption:
   6mW with Inputs Low
   120mW with Inputs High
- ◆ TTL/CMOS Input Compatible
- ♦ Low Rout Typically 4Ω
- Pin Equivalent to DS0026/DS0056, TSC426, SG1626/SG2626/SG3626

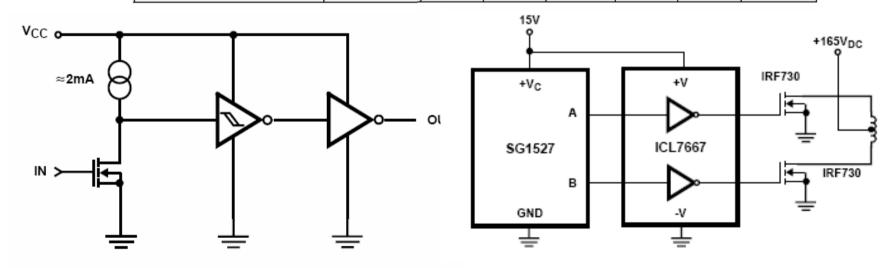
# ICL7667



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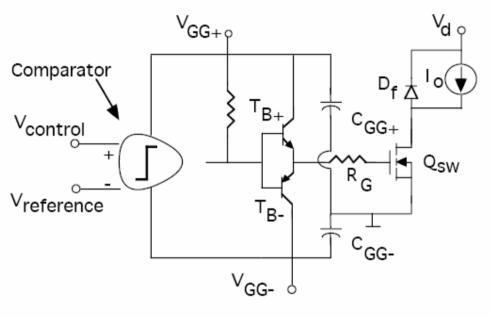
# ICL7667

SWITCHING SPECIFICATIONS							
Delay Time	T <sub>D2</sub>	35	50	-	-	60	ns
Rise Time	T <sub>R</sub>	20	30	-	-	40	ns
Fall Time	T <sub>F</sub>	20	30	-	-	40	ns
Delay Time	T <sub>D1</sub>	20	30	-	-	40	ns

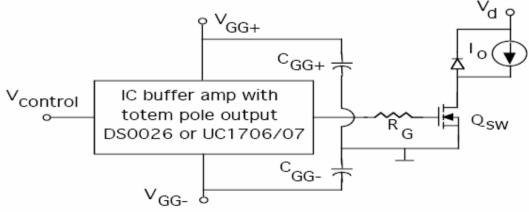




### **Bipolar DC-coupled Drive Circuit- MOSFET Example**



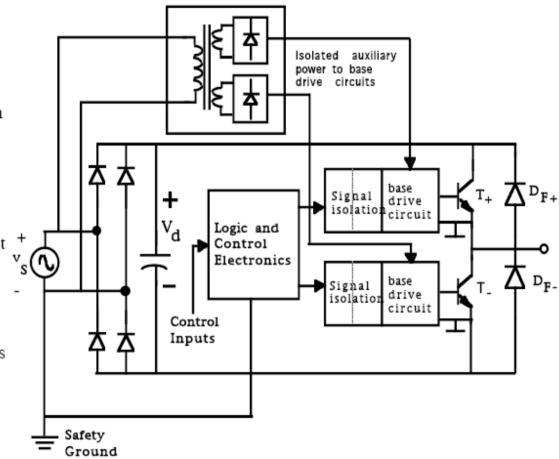
 Bipolar drive with substantial output current capability



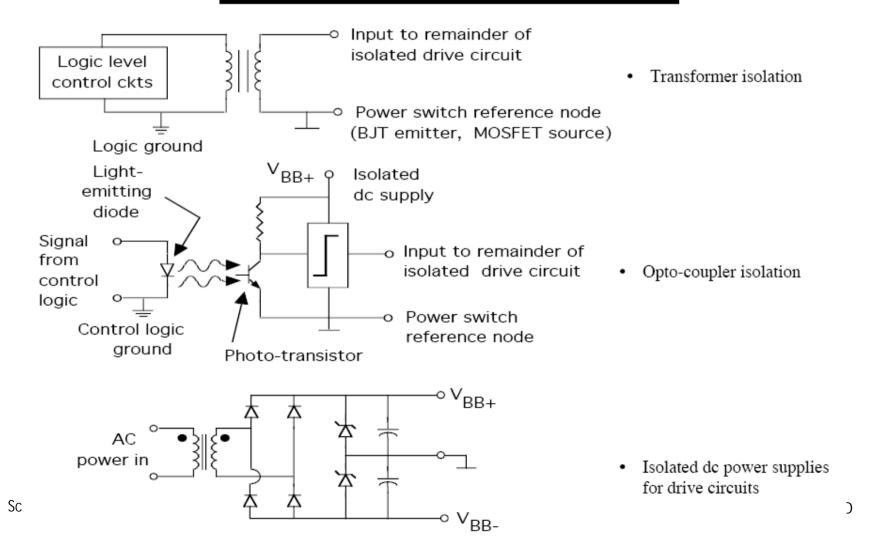
Simple bipolar drive circuit with moderate (1 amp)output current capability

## **Need for Electrical Isolation of Drive Circuits**

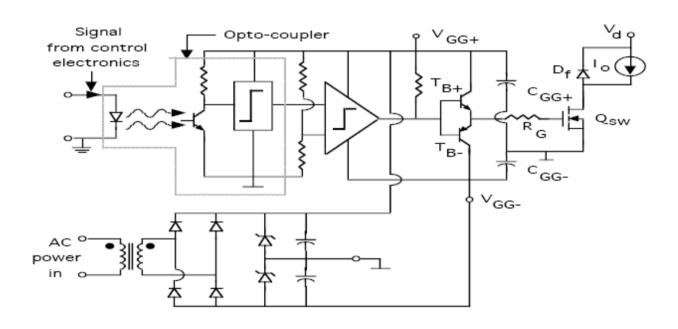
- Negative half cycle of v<sub>s</sub>(t) positive dc rail near safety ground potential. T<sub>j</sub> emitter potential large and negative with respect to safety and logic ground
- Postive half cycle of v<sub>s</sub>(t) negative dc rail near safety ground potential. T<sub>+</sub> emitter substantially positive with espect to safety ground if T<sub>-</sub> is off
- Variation in emitter potentials with respect to safety and logic ground means that electrical isolation of emitters from logic ground is needed.

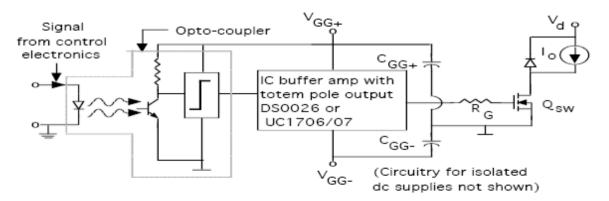


### **Methods of Control Signal Isolation**

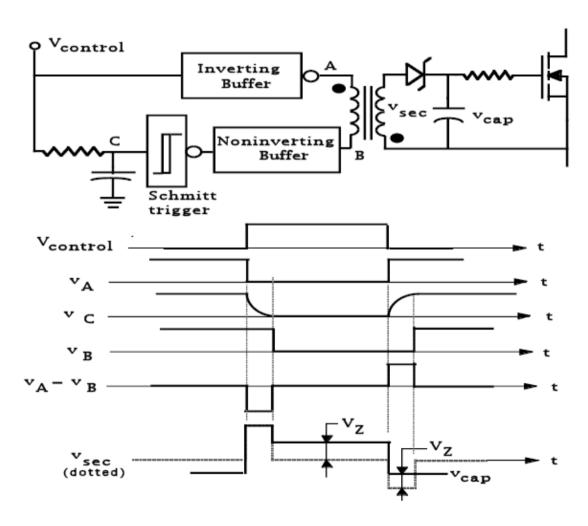






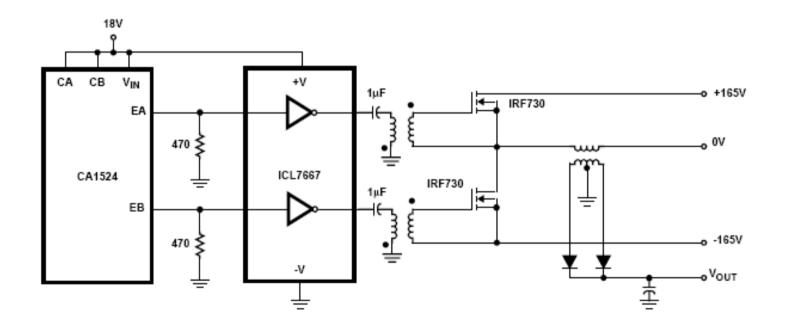


# Isolated Drive Without Auxiliary DC Supplies - MOSFET Example

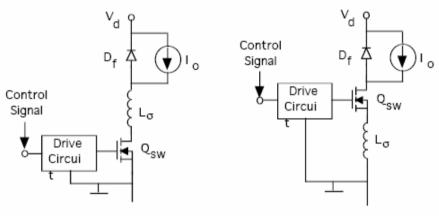


Zener diode voltage V<sub>Z</sub> must be less than negative pulse out of transformer secondary or pulse will not reach MOSFET gate to turn it off.



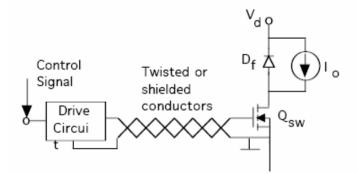


## Circuit/Component Layout Considerations

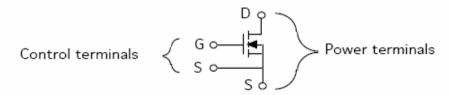


Prime consideration is minimizing stray inductance

- Stray inductance in series with high-voltage side of power device Q<sub>sw</sub> causes overvoltage at turnoff.
- Stray inductance in series with low-voltage side power device Q<sub>sw</sub> can cause oscill-ations at turnon and turn-off.
- One cm of unshielded lead has about 5 nH of series inductance.
- Keep unshielded lead lengths to an absolute minimum.



Use shielded conductors to connect drive circuit to power switch if there must be any appreciable separation (few cm or more) between them



Some power devices provided with four leads, two input leads and two power leads, to minimize stray inductance in input circuit.